

FIG. 1

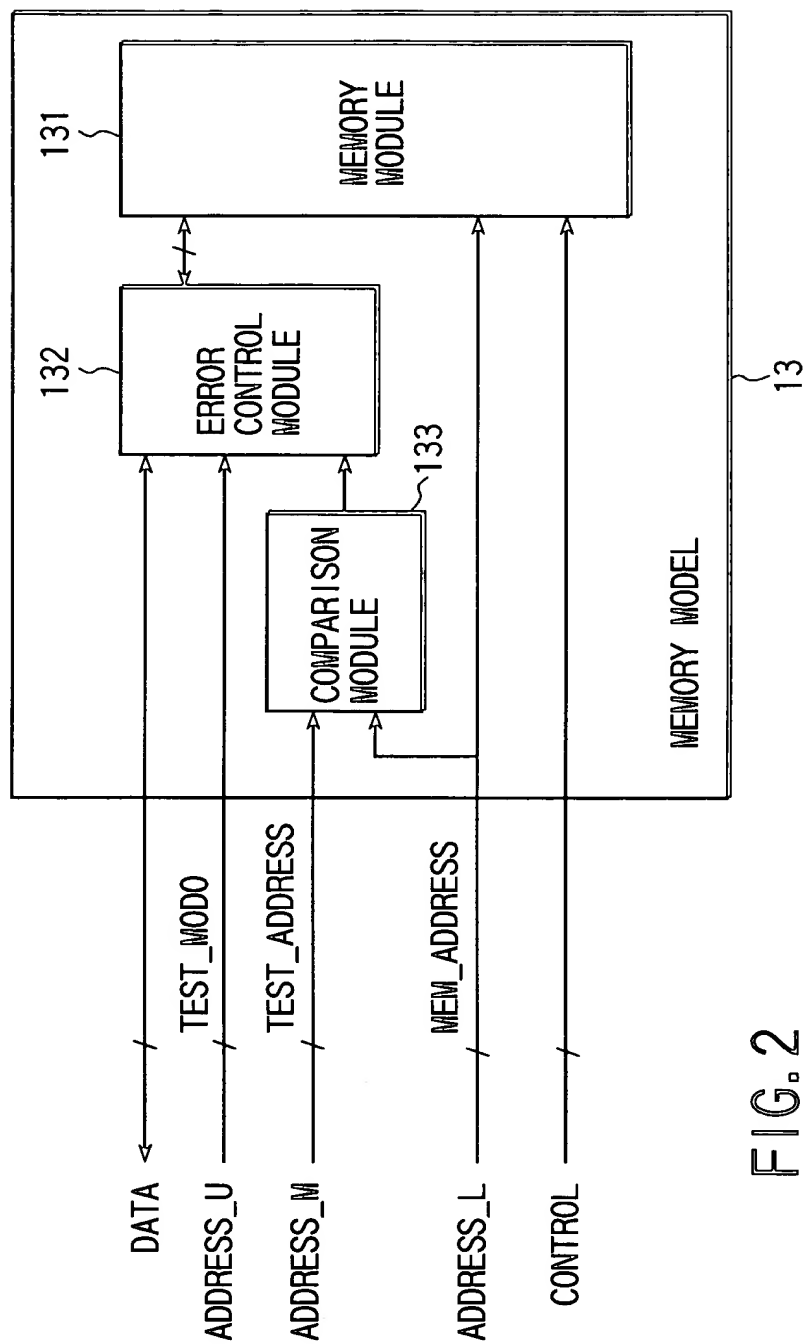


FIG. 2

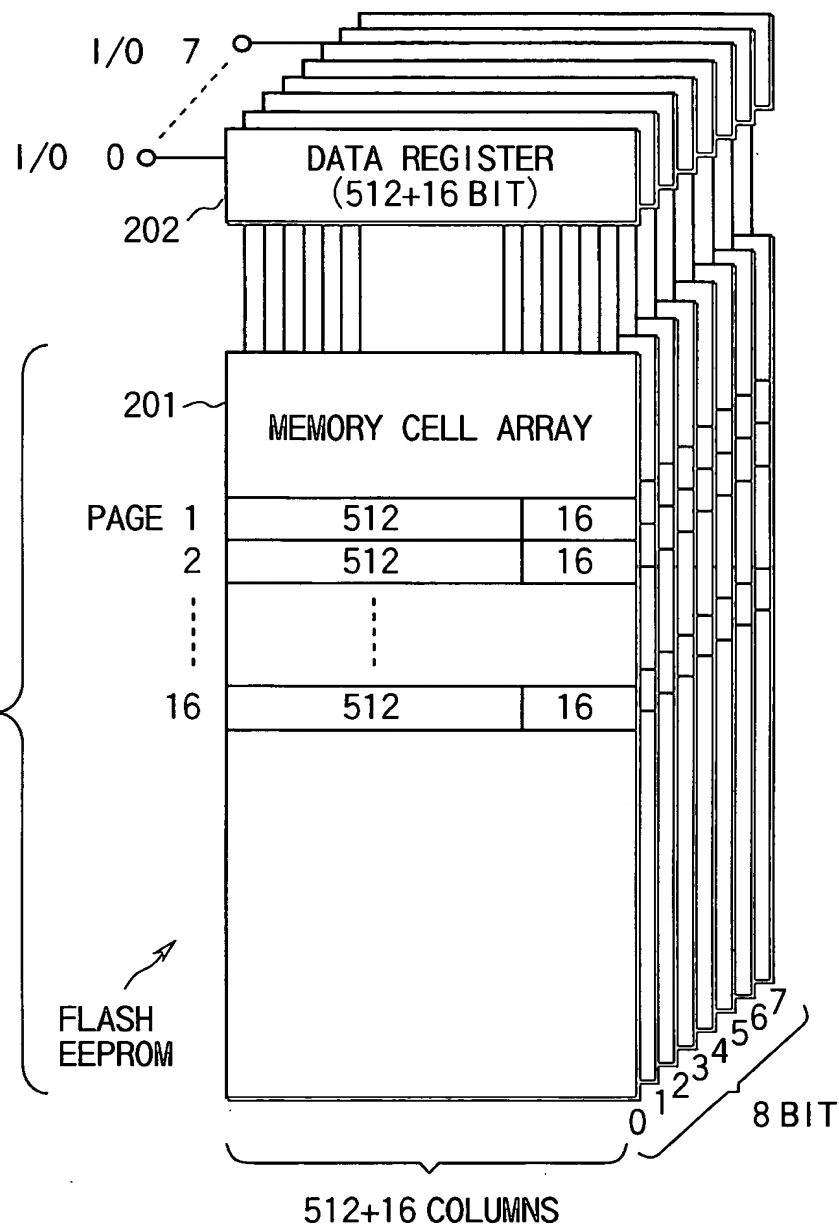


FIG. 3

PAGE 1	ECC
2	ECC
3	ECC
4	ECC

FIG. 4

	TMA		TEST_ADDR		PA	MA
NAND ADDRESS	23:22	21	20:12	11	10:09	08:00
NORMAL	00	*	*	*	PAGE SELECT	COLUMN ADDRESS
FAIL	FAIL MODE	*	FAIL ADDRESS	*	PAGE SELECT	COLUMN ADDRESS

FIG. 5

W/R	NAND ADDRESS <23:22>	MODE	FAIL DATA
WRITE	00	PASS	NORMAL
	01	1 BIT_FAIL	DATA <07> IS INVERT
	10	2 BIT_FAIL	DATA <07:06> IS INVERT
	11	3 BIT_FAIL	DATA <07:05> IS INVERT
READ	00	PASS	NORMAL
	01	1 BIT_FAIL	DATA <07> IS INVERT
	10	2 BIT_FAIL	DATA <07:06> IS INVERT
	11	3 BIT_FAIL	DATA <07:05> IS INVERT

FIG. 6

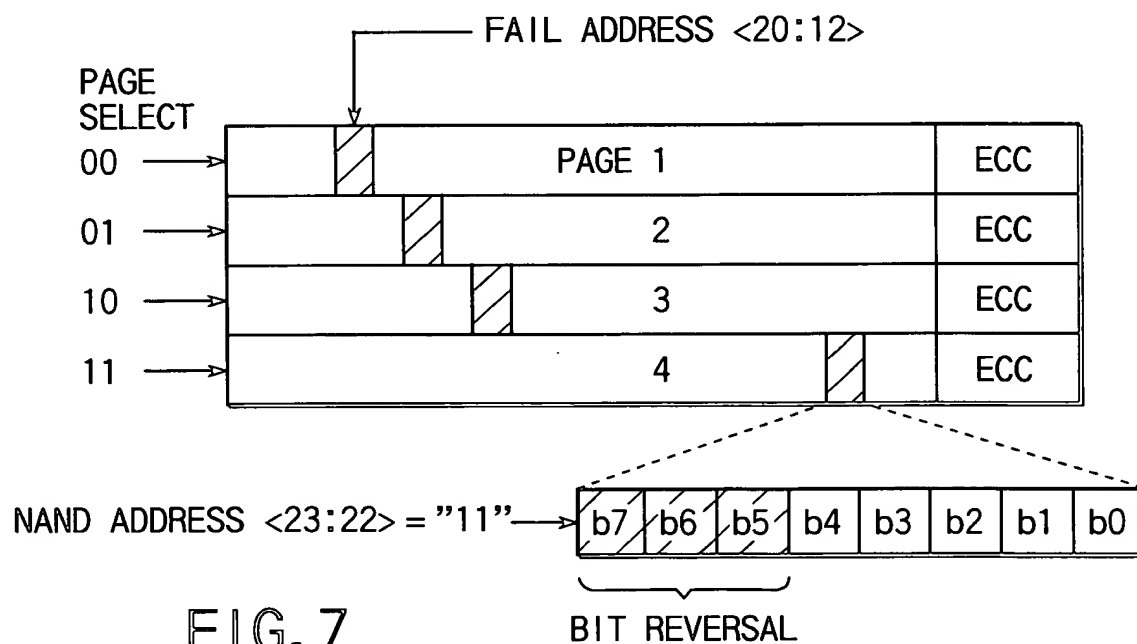


FIG. 7

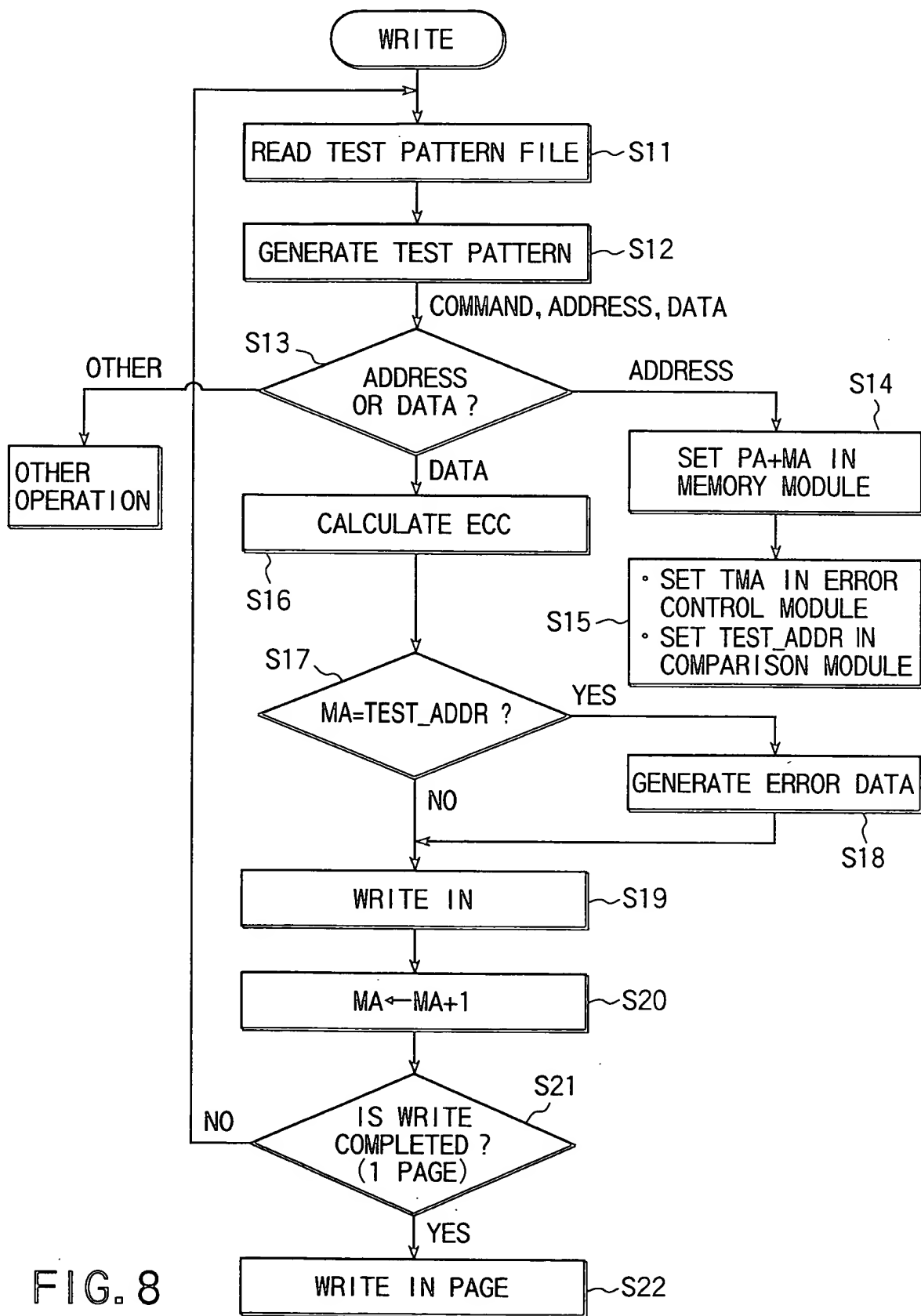


FIG. 8

